

WHAT IS CLAIMED IS:

1. A memory cell, comprising:
 - 5 a pair of complementary bitlines arranged along a first direction of the memory cell;
 - a first global ground supply line arranged above the pair of complementary bitlines along a second direction, which is perpendicular to the first
 - 10 direction; and
 - wherein a second global ground supply line either coupled to, or within, the memory cell is arranged along the first direction.
- 15 2. The memory cell as recited in claim 1, further comprising a wordline arranged above the pair of complementary bitlines and along the second direction.
3. The memory cell as recited in claim 2, further comprising:
 - 20 a first metal layer; and
 - a second metal layer arranged above the first metal layer.
4. The memory cell as recited in claim 3, wherein the first metal layer comprises the
25 complementary pair of bitlines, the second global ground supply line and a local interconnect line, and wherein the second metal layer comprises the first global ground supply line and the wordline.
5. The memory cell as recited in claim 3, further comprising a third metal layer
30 arranged above the second metal layer.

6. The memory cell as recited in claim 5, wherein the first metal layer comprises a local interconnect line, the second metal layer comprises the pair of complementary bitlines and the second global ground supply line, and the third metal layer comprises the wordline.
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7. The memory cell as recited in claim 6, further comprising a fourth metal layer arranged above the third metal layer and comprising the first global ground supply line.
8. The memory cell as recited in claim 6, wherein the third metal layer further
- 10 comprises the first global ground supply line.
9. The memory cell as recited in claim 8, wherein the memory cell is a single-port memory cell.
- 15 10. The memory cell as recited in claim 9, wherein the memory cell is a Static Random Access Memory (SRAM) memory cell.
11. The memory cell as recited in claim 8, further comprising:
- 20 an additional pair of complementary bitlines formed within the second metal layer and arranged along the first direction; and
- an additional wordline formed within the third metal layer and arranged along the second direction.
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12. The memory cell as recited in claim 11, wherein the memory cell is a dual-port memory cell.
13. The memory cell as recited in claim 12, wherein the memory cell is a Static
- 30 Random Access Memory (SRAM) memory cell.

14. A memory array, comprising:
- a plurality of bitlines traversing the memory array in a first direction;
- 5 a first plurality of global ground supply lines arranged above the plurality of bitlines and traversing the memory array in a second direction, which is perpendicular to the first direction; and
- a second plurality of global ground supply lines traversing the memory array in the
- 10 first direction.
15. The memory array as recited in claim 14, further comprising a plurality of word lines arranged above the plurality of bitlines and traversing the memory array in the second direction.
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16. The memory array as recited in claim 15, further comprising:
- a first metal layer;
- 20 a second metal layer arranged above the first metal layer; and
- a third metal layer arranged above the second metal layer.
17. The memory array as recited in claim 16, wherein the first metal layer comprises a
- 25 plurality of local interconnect lines, the second metal layer comprises the plurality of bitlines, and the third metal layer comprises the first plurality of global ground supply lines and the plurality of word lines.
18. The memory array as recited in claim 17, wherein a fourth metal layer is coupled
- 30 to the memory array above the third metal layer.

19. The memory array as recited in claim 18, wherein the second plurality of global ground supply lines are formed within the second metal layer.

20. The memory array as recited in claim 19, wherein formation of the second plurality of global ground supply lines within the second metal layer:

minimizes voltage fluctuations on a selected one of the first plurality of global ground supply lines;

substantially eliminates routing congestion within the fourth metal layer; and

provides horizontal shielding between bitlines of dissimilar ports, if the memory array comprises memory cells with more than one port.

21. The memory array as recited in claim 18, wherein the second plurality of global ground supply lines are formed within the fourth metal layer.

22. The memory array as recited in claim 21, wherein formation of the second plurality of global ground supply lines within the fourth metal layer:

minimizes voltage fluctuations on a selected one of the first plurality of global ground supply lines; and

minimizes an amount of area consumed by the memory array.

23. A system embedded within and/or arranged upon a single semiconductor chip, wherein the system comprises:

a memory array comprising a plurality of memory cells arranged in rows and columns, wherein the memory array comprises:

a plurality of bitlines arranged along a first direction of the memory array;

a first plurality of global ground supply lines arranged above the plurality
of bitlines along a second direction of the memory array, wherein
the second direction is perpendicular to the first direction; and

a second plurality of global ground supply lines arranged along the first
direction.

10 24. The system as recited in claim 23, wherein the memory array further comprises a
plurality of wordlines arranged above the plurality of bitlines along the second direction.

25. The system as recited in claim 24, wherein the plurality of wordlines and the first
plurality of global ground supply lines are formed within different metallization layers of
15 the system.

26. The system as recited in claim 24, wherein the plurality of wordlines are formed,
along with the first plurality of global ground supply lines, within an inter-level
metallization layer of the system.

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27. The system as recited in claim 26, wherein the system further comprises:

one or more subsystems; and

25 an upper-level metallization layer arranged above the inter-level metallization
layer, wherein the upper-level metallization layer comprises a plurality of
transmission lines for interconnecting the one or more subsystems and the
memory array.

28. The system as recited in claim 27, wherein the one or more subsystems are selected from a group comprising input/output devices, processing devices, control devices, power devices, communication devices, logic devices and additional memory arrays.

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29. The system as recited in claim 27, wherein the plurality of transmission lines are selected from a group comprising input/output (I/O) lines, clocking lines, intra-system signal lines, power supply lines, and ground supply lines.

10 30. The system as recited in claim 27, wherein the plurality of wordlines and the first plurality of global ground supply lines provide vertical shielding between the plurality of bitlines and the plurality of transmission lines.

31. The system as recited in claim 27, wherein the second plurality of global ground
15 supply lines are formed, along with the plurality of bitlines, within a lower-level metallization layer of the system, and wherein the lower-level metallization layer is arranged below the inter-level metallization layer.

32. The system as recited in claim 31, wherein the formation of the second plurality of
20 global ground supply lines within the lower-level metallization layer:

minimizes voltage fluctuations caused when a relatively large discharge current is
supplied to a selected one of the first plurality of global ground supply
lines;

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substantially eliminates routing congestion within the upper-level metallization
layer; and

provides horizontal shielding between bitlines of dissimilar ports, if the plurality
30 of memory cells comprise more than one port.

33. The system as recited in claims 31, wherein one or more of the first plurality of global ground supply lines are coupled to one or more of the second plurality of global ground supply lines to form a two-dimensional ground supply grid.
- 5 34. The system as recited in claim 27, wherein the second plurality of global ground supply lines are formed, along with the plurality of transmission lines, within the upper-level metallization layer.
35. The system as recited in claim 33, wherein the formation of the second plurality of
10 global ground supply lines within the upper-level metallization layer:
- minimizes voltage fluctuations caused when a relatively large discharge current is
supplied to a selected one of the first plurality of global ground supply
lines; and
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- minimizes an amount of area consumed by the system.
36. The system as recited in claims 34, wherein one or more of the first plurality of global ground supply lines are coupled to one or more of the second plurality of global
20 ground supply lines to form a two-dimensional ground supply grid.